Please amend the following paragraphs of the specification.

Page 1, Paragraph 2:

Filed on even date herewith are application serial Nos. 09/747,046 and 09/747,050, ~~(presently identified by Attorney Docket No's. RA-5339 and RA-5340)~~ which have substantially similar or identical disclosure to the disclosure contained herein but which claim different inventions.

Page 5, Paragraph 8:

~~Fig. 11. There is no Fig. 11.~~

Page 5, Paragraph 9:

Fig. ~~12~~ 11 is a block diagram of the logical component structure of another preferred embodiment of the invention.

Page 5, Paragraph 10:

Fig. ~~13~~ 12 is a block diagram of a part of a "2200" computer system connected to a collection system cable.

Page 5, Paragraph 11:

Fig. ~~14~~ 13 is a flow chart.

Page 17, Paragraph 2:

In another kind of system that this invention can perform tracing on, instead of a bus, processors themselves be tapped for data. In the 2200 architecture system from Unisys Corporation, such taps enable connections to two (2) processors having 50 bit wide busses each to be handled simultaneously with the equipment already described. In Fig. ~~13~~ 12, two (2) such processors P1 and P2 are illustrated having connections to half each of cable 17A, the cable that will lead into the collection system (not shown in this illustration). An

alignment scheme for such a system is described in greater detail with reference to Fig. 9, below, and it is important to mention here that a slightly different mode, we call dual mode, is used to handle this alignment. Activity of either processor acts as an alignment trigger, and the time stamp will have to be applied to both sets of signals through control block 209 as they are saved into the FIFO memory 207. The current Unisys 2200 instruction processor system currently requires an alignment scheme like that described with reference to Fig. 9.

Page 18, Paragraph 5:

In one aspect, the invention can provide throughput of aligned entries without compaction circuitry, which after all, is a separate function from managing the collection of the processor bus signals that arrive as input from input 201. Accordingly, such a system is illustrated in Fig. ~~12~~ 11 having sufficient preview logic 6a for alignment circuitry 203a to operate on previewed input reviewed against the alignment references provided by block 9a to preview circuitry 202a. Once aligned as entries, no further trigger review need be conducted (and in this embodiment trigger logic is not required), although the size of the FIFO may need to be greater, depending on the system under test and its characteristics in order to manage all the entries produced by the system under test without overflowing the high speed FIFO memory. Accordingly, the FIFO will in this simpler version of the inventive apparatus retain a time stamp for each entry in the same way as is described for the version with the compaction circuitry, and the PCI output logic will spool out the FIFO memory to the PCI bus 215 of the collector computer system in the same way too, through PCI output logic 208a.

Page ~~27~~ 26, Paragraph 1:

Refer now to Fig. 10 in which a flow diagram 40 of the collector system for tracing bus signals is outlined. The set up 41 is included here to indicate that the interposer and probe should be connected and tested and other arrangements

made to the system under test to establish the conditions for testing. The programmed selection should be selected 42 for the triggers if triggers are being used. The System Under Test (SUT) should be brought on-line and be running until it reaches the steady state 43 needed for testing purposes. At that point, the initiation 54 of the collection can be started. This initiation may require a sending of a signal to more than a single collector system if multiple parts of a multiprocessor are being used together for the results desired (whether from the same bus or from different busses) as will be explained below. Then the signals should be collected 44 into the preview pipeline and aligned to form entries. A time stamp should be generated based on the number of clock signals from initiation which clears the time stamp value in the time stamp register and is then set to begin collecting trace signals. If the user has set the apparatus to collect based on the first trigger or alignment reference to occur, the collection starts then. If in direct mode, the apparatus just begins collecting all cycles immediately. The time stamp sequence is restarted immediately on receipt of the initiation signal, and the time stamp value for the collected trace data should be collected 45 also. The time stamp value will be compacted and annexed 46 to the entry by logic so that it moves into the FIFO memory word associated with that entry. The triggers set by the operator (or possibly automatically in some cases) should be monitored in the output stream from the alignment logic in step 47. Compaction, if performed, is based on the trigger settings and should be performed in step 48. Then the compacted entries should be loaded into the high speed FIFO memory along with their respective time stamps 49. And these FIFO entries should be removed and passed on to the collector system bus at that bus's speed 51 by the FIFO output logic. The collector system memory should be set to handle a continuous stream of data at the system bus speed, up to however many entries will be needed to achieve an average steady state function for the test to be useful. The entries should be loaded into that memory 52, and then, when the trace is completed, that memory should be ~~pooled~~ flushed out to disk or other permanent memory for later study 53. It should be

clear from the discussion that in some embodiments there may be no alignment but compaction may be used, and vice versa. In some embodiments or settings, the user may desire not to use either, and a mode to allow that should be included in the apparatus.

Page 29, Paragraph 3:

Refer to Fig. ~~14~~ 13 in which the process 130 is illustrated. The operator would first set program all the systems through a console on the master or on each collector system. This set up would provide the various collector systems with appropriate settings. The operator would then wait for the SUT to come to steady state 131 before issuing a command to initiate collection to the master collector system 132. The master system then sends an initiation pulse to any slave systems 133, which also sends the initiation pulse command to the master system as described above. The trace can then begin 134 in accord with the settings in each collector system as described above.